



Avnet ANZ is currently presenting free Speedway workshops for Xilinx across Australia and New Zealand.

Avnet's SpeedWay workshops offer in-depth technical training providing you with practical "how-to" tutorials and labs on the latest Xilinx technology. Each workshop will challenge you with a hands-on experience using the newest Xilinx tools and development boards.

The Speedway workshop attendees are also entitled to discounts on the latest tools, limited to one set per company.

The courses on offer include:

1. General Design Courses:
  - Introduction to VHDL for FPGAs
  - Fundamentals of FPGA Design
  - Improving Design Performance
  - Advanced FPGA Configuration Techniques
2. Embedded Design Courses:
  - An Introduction to EDK and the MicroBlaze (Part 1)
  - An Introduction to EDK and the MicroBlaze (Part 2)
  - Embedded Debugging on MicroBlaze
  - Xilinx Embedded Software Development
  - Linux for MicroBlaze
3. DSP Design Courses:
  - Introduction to Xilinx AccelDSP
  - Xilinx System Generator for DSP: Part I – A Practical Guide

Course description and schedule are on the following pages.

To register your interest please email [XilinxANZ@Avnet.com](mailto:XilinxANZ@Avnet.com)

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General Design Courses	
<p><b>Introduction to VHDL for FPGA's</b></p>	<p>This introductory 1-day course will teach you the fundamentals of VHDL coding for FPGA's. The basic constructs of the VHDL language are reviewed with a special focus on implementation strategies for typical circuit functions. FPGA specific implementation issues and resource utilization will also be covered.</p> <p><b>Who Should Attend:</b> Design engineers looking to understand the basics of VHDL coding techniques.</p> <p><b>Prerequisites:</b> Digital design experience.</p> <p><b>Contact:</b> <a href="mailto:XilinxANZ@Avnet.com">XilinxANZ@Avnet.com</a></p>
<p><b>Fundamentals of FPGA Design</b></p>	<p>This introductory 1 course will teach digital designers the basics of designing an FPGA-based solution. Using the latest Xilinx ISE development tools, engineers will learn the basic FPGA development process of design entry, simulation, constraining, synthesis, implementation, timing analysis, and design download. Through a combination of lectures and hands-on labs, each step of the process will be explained and re-enforced through easy to follow step-by-step lab exercises.</p> <p><b>Who Should Attend:</b> Digital design engineers new to FPGA design and/or the Xilinx ISE tools.</p> <p><b>Prerequisites:</b> Digital design experience and general knowledge of FPGA's and HDLs (VHDL or Verilog) is required.</p> <p><b>Contact:</b> <a href="mailto:XilinxANZ@Avnet.com">XilinxANZ@Avnet.com</a></p>
<p><b>Improving Design Performance</b></p>	<p>This course will teach FPGA designers how to analyze design performance by using timing reports in order to achieve timing closure. Using the new Xilinx ISE 9.2 development tools, engineers will learn techniques for making path-specific timing constraints, creating timing groups and specifying external data and clock relationship for the timing on paths to and from the FPGA I/O pins by using the Xilinx Constraints Editor.</p> <p><b>Who Should Attend:</b> FPGA designers who want to improve their designs speed and resource utilization.</p> <p><b>Prerequisites:</b> Familiarity with Xilinx FPGA design and the ISE tools.</p> <p><b>Contact:</b> <a href="mailto:XilinxANZ@Avnet.com">XilinxANZ@Avnet.com</a></p>

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### General Design Courses

#### Advanced FPGA Configuration Techniques

At power up, Xilinx FPGA's go through a configuration step, where their design identities are loaded into the FPGA SRAM. Recent advances in this area include the ability to configure from multiple design images stored in industry standard serial or parallel flash as well as configuring from on-chip flash memory. This course explains how to take advantage of these features, teaching the basic configuration techniques using serial and parallel flash. You will also look at some advanced options of running a multi-boot application with multiple design images. The concluding experiment of the day will show you how to take advantage of these features to design a fail-safe system capable of self-updating bitstreams over Ethernet.

**Who Should Attend:** Hardware engineers interested in taking advantage of advanced configuration techniques with Spartan-3A/3AN/3ADSP.

**Prerequisites:** Familiar with ISE Project Navigator (including iMPACT). Must know either VHDL or Verilog. Previous experience with Xilinx Platform Studio and MicroBlaze is helpful but not required.

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### Embedded Design Courses

#### An Introduction to EDK and the MicroBlaze (Part 1)

The growth of FPGA-based embedded processors presents both opportunity and challenges for current FPGA designers. This half-day, hands-on workshop will teach you how to architect a MicroBlaze® based system using the latest Embedded Development Kit (EDK 9.2i) from Xilinx. Based on the Xilinx MicroBlaze v7.0 processor core, this class covers the details of defining your hardware system, implementing the design, incorporating application code, and booting. At the end of the course, students will take home sufficient knowledge to build and run their own MicroBlaze based systems.

**Who Should Attend:** FPGA designers interested using the MicroBlaze processor core in the Xilinx FPGA's.

**Prerequisites:** Knowledge of the Xilinx ISE implementation tools and general knowledge of microprocessors and embedded C programming.

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#### An Introduction to EDK and the MicroBlaze (Part 2)

The explosive growth of FPGA-based embedded processing is occurring today. The high-performance, soft-processor MicroBlaze core from Xilinx is leading the way, along with the newest EDK 9.2i release of embedded processing development tools. This half-day, hands-on workshop will walk students through the process of designing a custom peripheral for the MicroBlaze processor. The workshop will also teach students how to debug a MicroBlaze based system using the GNU debug environment. Through a combination of lecture and hands-on labs, the student will gain the practical experience and know-how that will save weeks of time.

**Who Should Attend:** Hardware designers interested in FPGA-based embedded processing.

**Prerequisites:** Knowledge of the Xilinx ISE implementation tools and general knowledge of microprocessors and embedded C programming.

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### Embedded Design Courses

#### Embedded Debugging on MicroBlaze

Debugging is an integral part of any embedded systems development. FPGA-based embedded processors systems add the additional challenges of hardware that is just as malleable as the software and custom peripherals with limited visibility outside of the FPGA. Through a combination of lectures and hands-on labs this half-day, hands-on workshop will introduce the Xilinx Software Development Kit (SDK) software tools, the ChipScope Pro logic analyzer and the cross triggering capability between the two that can aid in debugging system or 'platform' level issues. Labs will take attendees through importing applications into the SDK and connecting to the GDB software debugger via JTAG interface to the processor Hardware Debug Module. ChipScope Pro Integrated Bus Analyzer (IBA) and Integrated Logic Analyzer (ILA) cores will be discussed and students will use the Xilinx Platform Studio (XPS) Debug Configuration Wizard to add the cores to a MicroBlaze embedded processor design. The combination of the SDK and ChipScope Pro tools will be used to debug the processor and custom peripherals and software.

**Who Should Attend:** Hardware and Software Engineers that will be developing and debugging FPGA embedded processor based systems.

**Prerequisites:** An understanding of embedded systems is required. Prior experience with the Xilinx EDK implementation tools is recommended.

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### Embedded Design Courses

#### Xilinx Embedded Software Development

FPGA-based embedded processors present a new set of challenges and opportunities for embedded software developers. This half-day, hands-on workshop is specifically targeted to embedded software engineers who understand the basic concepts of embedded programming, but are unfamiliar with the FPGA-based embedded processor development flow. Through a combination of lectures and hands-on labs this course covers the Xilinx Embedded Development Kit (EDK) with the supporting applications, generating a board support package, software debugging, manipulating program memory space, and implementing a stand-alone boot sequence. The labs and lecture are based the MicroBlaze version 7 soft-core processor.

**Who Should Attend:** Embedded software engineers interested in FPGA-based embedded processing.

**Prerequisites:** Familiarity with general embedded software development and C programming. Experience with FPGA design tools is not required.

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## Embedded Design Courses

### Linux for MicroBlaze

Are you interested in using Linux on your next Xilinx® MicroBlaze™ 7 design? Tired of trying to wade through the jumble of information in the open source world? Confused about whether or not you need an MMU? Then attend the new Avnet SpeedWay Workshop and we'll show you all the things you need to know to get started with the 2.6 kernel, with or without the MMU.

Linux for MicroBlaze is centered around two new exciting developments from the embedded Linux GPL world and from Xilinx. Starting with the 2.6.13 kernel much of the work sponsored by the uClinux project was merged with the mainline Linux kernel, allowing kernel code based on the standard kernel.org source tree to be built for an MMU-less processor such as MicroBlaze 6 and earlier versions. Also, Xilinx has recently announced MicroBlaze 7, which allows the soft processor to be configured with an MMU as well. So now there are several possible combinations to consider, each with their own advantages and challenges.

This all-day introductory class will teach you the relationship between the flexible FPGA platform and the Linux operating system. We show you how to build the hardware from the ground up, using the Xilinx Spartan-3A™ DSP 1800A Starter Kit. Next, it's all about getting the software files you need for development, configuring the kernel, and building and executing on the hardware platform. Your design includes a TCP/IP network, a web server and set up of your system to boot from power up using the open-source defacto standard U-Boot. With the Linux kernel in place, you can see how to add your own applications on top of the kernel, and how to debug them on the board over the network connection with GDB.

**Who Should Attend:** Software engineers and hardware engineers with software experience who need to upgrade their embedded system from a standalone software environment. If you need to run multiple concurrent applications and would benefit from features such as a TCP/IP protocol stack, comprehensive boot loader and a file system for RAM or ROM, then you should consider this course.

**Prerequisites:** This course is recommended for hardware and software developers interested in MicroBlaze processor development with Linux. Familiarity with the MicroBlaze soft-processor core and Xilinx Platform Studio™ is recommended. Prior attendance of the Introduction to EDK and MicroBlaze Part 1 and 2 SpeedWay is encouraged.

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2007-2008  
SpeedWay Design Workshops™

DSP Design Courses	
<p><b>Introduction to Xilinx AccelDSP</b></p>	<p>Many signal processing applications require matrix inversion to solve a system of equations in real-time. This ½ day course will feature FPGA-based matrix operations in a variety of applications such as mobile WiMAX, automotive sonar, GPS, beamforming (medical and wireless), radar, and image processing. Hands on labs will use AccelDSP to leverage MATLAB, the native floating point simulation language, to explore hardware ramifications while implementing optimal fixed-point FPGA designs.</p> <p><b>Who Should Attend:</b> MATLAB algorithm designers and their FPGA hardware colleagues seeking the extra performance of Xilinx FPGA's.</p> <p><b>Prerequisites:</b> Knowledge of MATLAB. Familiarity with Xilinx FPGA's useful.</p> <p><b>Contact:</b> <a href="mailto:XilinxANZ@Avnet.com">XilinxANZ@Avnet.com</a></p>
<p><b>Xilinx System Generator for DSP: Part I – A Practical Guide</b></p>	<p>System Generator for DSP is the industry's leading high-level tool for designing high-performance DSP systems using Xilinx FPGA's. This 1/2-day, hands-on technical session will introduce the System Generator model-based abstractions that enable you to quickly develop high performance DSP systems, using system modeling and automatic code generation from Simulink and MATLAB® (The MathWorks, Inc.). Key components include model creation using Simulink with highly optimized DSP blocks for Xilinx FPGA's, model simulation, hardware and software co-simulation, and finally integrating a custom System Generator design into a larger HDL-based project using the Xilinx ISE™ implementation tools.</p> <p><b>Who Should Attend:</b> Any Hardware or DSP system designer who needs to implement complex, high performance DSP algorithms in a Xilinx FPGA using intuitive, graphical-based design tools.</p> <p><b>Prerequisites:</b> Basic understanding of fundamental DSP concepts will be helpful. Prior experience with the Xilinx ISE™ implementation tools will also be useful.</p> <p><b>Contact:</b> <a href="mailto:XilinxANZ@Avnet.com">XilinxANZ@Avnet.com</a></p>

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Location	Course	Date
Adelaide	Fundamentals of FPGA Design	29-Apr-08
	An Introduction to EDK and MicroBlaze (Part 1 & 2)	30-Apr-08
	Embedded Debugging on MicroBlaze	01-May-08
	Xilinx Embedded Software Development	01-May-08
Auckland	Introduction to VHDL for FPGAs	11-Feb-08
	Fundamentals of FPGA Design	25-Feb-08
	Xilinx System Generator for DSP – A Practical Guide	14-Mar-08
	An Introduction to EDK and MicroBlaze (Part 1 and 2)	19-May-08
Brisbane	Introduction to VHDL for FPGAs	05-Feb-08
	Fundamentals of FPGA Design	12-Feb-08
	Improving Design Performance	19-Feb-08
	Advanced FPGA Configuration Techniques	26-Feb-08
	An Introduction to EDK and MicroBlaze (Part 1 and 2)	04-Mar-08
	Xilinx System Generator for DSP – A Practical Guide	22-Apr-08
	Introduction to Xilinx AccelDSP	29-Apr-08
Canberra	Introduction to VHDL for FPGAs	13-May-08
	Fundamentals of FPGA Design	14-May-08
	Xilinx System Generator for DSP – A Practical Guide	15-May-08
	Introduction to Xilinx AccelDSP	16-May-08
Christchurch	Introduction to VHDL for FPGAs	15-Feb-08
	Fundamentals of FPGA Design	28-Feb-08
	Xilinx System Generator for DSP – A Practical Guide	20-Mar-08
	An Introduction to EDK and MicroBlaze (Part 1)	23-May-08
	An Introduction to EDK and MicroBlaze (Part 2)	23-May-08
Melbourne	Introduction to VHDL for FPGAs	30-Jan-08
	Fundamentals of FPGA Design	31-Jan-08
	Improving Design Performance	06-Feb-08
	Advanced FPGA Configuration Techniques	13-Feb-08
	An Introduction to EDK and MicroBlaze (Part 1)	20-Feb-08
	An Introduction to EDK and MicroBlaze (Part 2)	20-Feb-08
	Embedded Debugging on MicroBlaze	27-Feb-08
	Xilinx Embedded Software Development	27-Feb-08
	Implementing uCLinux on MicroBlaze	05-Mar-08
	Introduction to Xilinx AccelDSP	12-Mar-08

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Perth	Fundamentals of FPGA Design	22-Apr-08
	Xilinx System Generator for DSP – A Practical Guide	23-Apr-08
	Introduction to Xilinx AccelDSP	24-Apr-08
Sydney	Introduction to VHDL for FPGAs	18-Mar-08
	Fundamentals of FPGA Design	19-Mar-08
	Improving Design Performance	26-Mar-08
	An Introduction to EDK and MicroBlaze (Part 1 and 2)	01-Apr-08
	An Introduction to EDK and MicroBlaze (Part 1 and 2)	03-Apr-08
	Xilinx System Generator for DSP – A Practical Guide	06-May-08
	Introduction to Xilinx AccelDSP	07-May-08
Wellington	Introduction to VHDL for FPGAs	13-Feb-08
	Xilinx System Generator for DSP – A Practical Guide	18-Mar-08
	Introduction to Xilinx AccelDSP	06-May-08
	An Introduction to EDK and MicroBlaze (Part 1 and 2)	21-May-08

Venues of where courses are run:

Adelaide:	Avnet EM Pty Ltd Office Unit 1, 561-567 Port Rd West Croydon Adelaide SA 5008	Auckland:	Avnet EM Pty Ltd Office Level 3, Building A 4 Pacific Rise Mt. Wellington Auckland 1060
Brisbane:	Australian Microelectronics Centre Brisbane Technology Park Cnr Logan & Miles Platting Rds Eight Mile Plains Brisbane	Canberra:	TBA
Perth:	TBA	Christchurch:	TBA
Sydney:	Avnet EM Pty Ltd Office Suite 1, Level 6 111 Phillip Street Parramatta, NSW 2150	Melbourne:	Avnet EM Pty Ltd Office Unit 2 17-19 Melrich Road Bayswater, VIC 3153
		Wellington:	TBA

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